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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/678,163	10/02/2000	Jerry D. Kline	1303-1008	4116

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EXAMINER
LEE, HSIEN MING

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/678,163	KLINE, JERRY D.	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-41 are rejected under 35 U.S.C. 102(e) as being anticipated by Jerry Kline (US 6,537,831)

The applied reference has a *common inventor* with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In re claims 1, 18, 35 and 36, Kline expressly teaches the claimed method for selecting components for a matched set and the claimed matches set of integrated circuit chips by the claimed method, comprising the steps of:

- electrically and mechanically coupling a semiconductor wafer 24 having a plurality of integrated circuit chips 38 to an interposer 12 to form a wafer-interposer assembly 10, wherein the chips 38 are digital devices, analog devices, RF devices or mixed signal devices (Fig. 1 and col. 6, lines 46-50);

- simultaneously testing at least two of the integrated circuit chips 38 of the semiconductor wafer 24 (Figs. 6-7 and col. 6, lines 32-36) to determine inclusion in the matched set (col.3, lines 23-30);
- dicing the wafer-interposer assembly 10 into a plurality of chip assemblies (Fig.8 and col. 3, lines 23-26);
- selecting or sorting at least two of the chip assemblies corresponding to the at least two of the integrated circuit chips determined for inclusion in the matched set based upon the inclusion determinations performed during the simultaneous testing of pairs of the integrated circuit chips 38 (col. 3, lines 29-34; col.6, lines 32-50,col. 15,claim 24); and
- electrically coupling at least two of the chip assemblies corresponding to a sorted pair of the integrated circuit chip 38 onto a substrate, thereby assembling the matched set (col.15, claim 24).

In re claims 2-6 and 19-23, Kline also teach that the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously testing groups of the integrated circuit chips together to identify which groups of integrated circuit chips perform best together for inclusion in a selected number of high performance matched sets (i.e. claims 2 and 19) (col. 3,lines 5-13); to grade the groups of integrated circuit chips for performance such that the overall performance of matched sets assembled from the chip assemblies is maximized (i.e. claims 3 and 20)(col. 3,lines 5-13); to identify the compatibility of individual integrated circuit chips with one another (i.e. claims 4 and 21); to identify which individual integrated circuit chips are incompatible with one another (i.e. claims 5 and 22); and to simultaneously test at least two

of the integrated circuit chips for performance over a range of temperatures (i.e. claims 6 and 23)(col. 3, lines 5-45; col. 13, claims 2, 6 and 7; col. 14, claims 14 and 18).

In re claims 7-13 and 24-30, Kline also teaches that the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously performing burn-in testing of the at least two of the integrated circuit chips (i.e. claims 7 and 24); simultaneously vibrating the at least two of the integrated circuit chips (i.e. claims 8 and 25); simultaneously testing the at least two of the integrated circuit chips for leakage currents (i.e. claims 9 and 26); simultaneously testing the at least two of the integrated circuit chips for offset voltages (i.e. claims 10 and 27); simultaneously testing the at least two of the integrated circuit chips for gain tracking (i.e. claims 11 and 28); simultaneously testing the at least two of the integrated circuit chips for bandwidth (i.e. claims 12 and 29); simultaneously testing the at least two of the integrated circuit chips for speed grades (i.e. claims 13 and 30) (col. 13, claims 3-5; col.14, claims 14-17).

In re claims 14-17, 31-34 and 37-40, Kline also teaches that the integrated circuit chips of the semiconductor wafer are digital devices, analog devices, RF devices and mixed signal devices (col. 13, claims 8-10).

In re claim 41, Kline further teaches a third chip assembly diced from the wafer-interposes assembly, the third chip assembly including a third integrated circuit chip from the wafer, the first, second and third integrated circuit chips being previously simultaneously tested as part of the wafer-interposes assembly, the third chip assembly electrically coupled to the substrate because Kline teaches a plurality of wafer-interposes assemblies and plurality of integrated circuit chips being simultaneously tested and coupled to the substrate as shown in Figs. 6-11.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6,483,330, US 6,483,043 and US 6,392,428 teach the claimed subject matter.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Hsien-Ming Lee
Examiner
Art Unit 2823

June 20, 2003